//testbench

module fbcountertb;

reg clk, reset;

wire [3:0] y;

fbcounter uut(.clk(clk), .reset(reset), .y(y));

initial begin

$dumpfile ("fbcounter.vcd");

$dumpvars (1, fbcountertb);

clk = 0;

reset = 0;

forever #5 clk = ~clk;

end

initial begin

#10 reset =1;

#10 reset =0;

#200

$finish;

end

endmodule

//design

module fbcounter(clk, reset, y);

input clk, reset;

output [3:0] y;

reg [3:0] y;

always @(posedge clk) begin

if(reset)

y = 4'b0000;

else

y = y + 4'b0001;

end

endmodule